CLAIMS

What is claimed is:

1. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure, coupled to a first of said ingress/egress point and a first one of said mediums, including a first FIFO storage structure to stage undiverted ones of a first plurality of egress packets, and first undiverted egress packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flushes of said first FIFO storage structure; and

a second buffering structure, coupled to a second of said ingress/egress point and a second one of said mediums, including a second FIFO storage structure to stage undiverted ones of a second plurality of egress packets, and second undiverted egress packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure.

2. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an egress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said first FIPO storage structure.

3. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

4. The apparatus of claim 3, wherein said first undiverted egress packet write drop logic further sets a bad egress packet bit to denote for a downstream processor that an immediately preceding egress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

5. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from the SOP of the egress packet to be dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

6. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

7. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is no longer in the first FIFO storage structure, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

8. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said first FIPO storage structure.

9. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and

if so, invalidating remaining words of the egress packet,

to effectuate a head flush of said first FIPO storage structure.

10. The apparatus of claim 1, wherein said first undiverted egress packet drop logic comprises first undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped has already been read out of the first FIFO storage structure, and

if so, invalidating an EOP indicator of a current word,

to effectuate a head flush of said first FIPO storage structure.

11. The apparatus of claim 1, wherein

said first plurality of FIFO storage structures further comprises a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said first plurality of egress packets; and

said first associated packet diversion and insertion logic further includes a diverted egress packet write drop logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

12. The apparatus of claim 11, wherein said diverted egress packet write drop logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop logic effectuates a tail flush of the first FIFO storage structure.

13. The apparatus of claim 1, wherein said first buffering structure further comprises a third FIFO storage structure to stage undiverted ones of a first plurality of ingress packets, and first undiverted ingress packet drop logic to selectively effectuate head or tail flushes of said third FIFO storage structure.

14. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the third FIFO storage structure to point to a location in the third FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said third FIPO storage structure.

15. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the third FIFO storage structure to point to a location in the third FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the third FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said third FIPO storage structure.

16. The apparatus of claim 15, wherein said first undiverted ingress packet write drop logic further sets a bad ingress packet bit to denote for a system-side interface that an immediately preceding ingress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

17. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the third FIFO storage structure, and whether the SOP is greater than a read pointer associated with the third FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the third FIFO storage structure with an address that is of a second predetermined distance from the SOP of the ingress packet to be dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said third FIPO storage structure.

18. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the third FIFO storage structure, and whether the SOP is less than a read pointer associated with the third FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the third FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the third FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said third FIPO storage structure.

19. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is no longer in the third FIFO storage structure, and

if so, reloads a write pointer associated with the third FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the third FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said third FIPO storage structure.

20. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to an underflow condition of said third FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said third FIPO storage structure.

21. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the third FIFO storage structure, and

if so, invalidating remaining words of the ingress packet to be dropped,

to effectuate a head flush of said third FIPO storage structure.

22. The apparatus of claim 13, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped has already been read out of the third FIFO storage structure, and

if so, invalidating an EOP indicator of a current word,

to effectuate a head flush of said third FIPO storage structure.

23. The apparatus of claim 13, wherein said first buffering structure comprises a fourth FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets; and

diverted ingress packet write drop logic coupled to the fourth FIFO storage structure to effectuate a tail flush of the fourth FIFO storage structure.

24. The apparatus of claim 23, wherein said diverted ingress packet write drop logic effectuates a tail flush of the fourth FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop logic effectuates a tail flush of the third FIFO storage structure.

25. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch routing paths of packets received through mediums coupled to the ingress/egress points;

a first buffering structure, coupled to a first of said ingress/egress points and a first of said mediums, including a first FIFO storage structure to stage undiverted ones of a first plurality of ingress packets, and first undiverted ingress packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flushes of said first FIFO storage structure; and

a second buffering structure, coupled to a second of said ingress/egress points and a second of said mediums, including a second FIFO storage structure to stage undiverted ones of a second plurality of ingress packets, and second undiverted ingress packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flushes of said second FIFO storage structure.

26. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to an overflow condition of said third FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

27. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

28. The apparatus of claim 27, wherein said first undiverted ingress packet write drop logic further sets a bad ingress packet bit to denote for a system-side interface that an immediately preceding ingress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

29. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from the SOP of the ingress packet to be dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

30. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

31. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is no longer in the first FIFO storage structure, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said first FIPO storage structure.

32. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

33. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and

if so, invalidating remaining words of the ingress packet to be dropped,

to effectuate a head flush of said first FIPO storage structure.

34. The apparatus of claim 25, wherein said first undiverted ingress packet drop logic comprises first undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped has already been read out of the first FIFO storage structure, and

if so, invalidating an EOP indicator of a current word,

to effectuate a head flush of said first FIPO storage structure.

35. The apparatus of claim 25, wherein said first buffering structure further comprises

a third FIFO storage structure coupled to said first medium to stage diverted ones of said first plurality of ingress packets; and

diverted ingress packet write drop logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

36. The apparatus of claim 35, wherein said diverted ingress packet write drop logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop logic effectuates a tail flush of the first FIFO storage structure.

37. A networking apparatus comprising:

a switching fabric including a plurality of ingress/egress points to switch packets received through mediums coupled to the ingress/egress points; and

a buffering structure including

a first FIFO storage structure, coupled to a first of said ingress/egress points and a first of said mediums, to stage undiverted ones of a first plurality of ingress packets, and undiverted ingress packet drop logic to

selectively effectuate head or tail flushes of said first FIFO storage structure, and

a second FIFO storage structure, coupled to said first ingress/egress point and said first of said mediums, to stage undiverted ones of a first plurality of egress packets, and undiverted egress packet drop logic to selectively effectuate head or tail flushes of said second FIFO storage structure.

38. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a SOP location of an ingress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

39. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to an overflow condition of said first FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the first FIFO storage structure to point to a location in the first FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said first FIPO storage structure.

40. The apparatus of claim 39, wherein said undiverted ingress packet write drop logic further sets a bad ingress packet bit to denote for a system-side interface that an immediately preceding ingress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

41. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is greater than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from the SOP of the ingress packet to be dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said first FIPO storage structure.

42. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the first FIFO storage structure, and whether the SOP is less than a read pointer associated with the first FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

43. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet write drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is no longer in the first FIFO storage structure, and

if so, reloads a write pointer associated with the first FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the first FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said first FIPO storage structure.

44. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet read drop logic, which, in response to an underflow condition of said first FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said first plurality of ingress packets to denote to a system-side interface that a current ingress packet is bad, to effectuate a head flush of said first FIPO storage structure.

45. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped is still in the process of being read out of the first FIFO storage structure, and

if so, invalidating remaining words of the ingress packet to be dropped,

to effectuate a head flush of said first FIPO storage structure.

46. The apparatus of claim 37, wherein said undiverted ingress packet drop logic comprises undiverted ingress packet read drop logic, which, in response to a drop ingress packet control signal, while operating under a first protocol,

determines whether a SOP of an ingress packet to be dropped has already been read out of the first FIFO storage structure, and

if so, invalidating an EOP indicator of a current word,

to effectuate a head flush of said first FIPO storage structure.

47. The apparatus of claim 37, wherein said buffering structure further comprises

a third FIFO storage structure coupled to said first medium to stage diverted ones of said plurality of ingress packets; and

diverted ingress packet write drop logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

48. The apparatus of claim 47, wherein said diverted ingress packet write drop logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted ingress packet write drop logic effectuates a tail flush of the first FIFO storage structure.

49. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet write drop logic, which, in response to an

overflow condition of said second FIFO storage structure, while operating under a first protocol,

reloads a write pointer associated with the second FIFO storage structure to point to a location in the second FIFO storage structure that is of a predetermined offset from a SOP location of an egress packet being dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said second FIPO storage structure.

50. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet write drop logic, which, in response to an overflow condition of said second FIFO storage structure while operating under a first protocol,

reloads a write pointer associated with the second FIFO storage structure to point to a location in the second FIFO storage structure that is of a predetermined offset from a location pointed to by a read pointer associated with the second FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said second FIPO storage structure.

51. The apparatus of claim 50, wherein said undiverted egress packet write drop logic further sets a bad egress packet bit to denote for a downstream processor that an immediately preceding egress packet was aborted, while writing an EOP at the location being pointed to by the reloaded write pointer.

52. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the second FIFO storage structure, and whether the SOP is greater than a read pointer associated with the second FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the second FIFO storage structure with an address that is of a second predetermined distance from the SOP of the egress packet to be dropped, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said second FIPO storage structure.

53. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the second FIFO storage structure, and whether the SOP is less than a read pointer associated with the second FIFO storage structure by a first predetermined distance, and

if so, reloads a write pointer associated with the second FIFO storage structure with an address that is of a second predetermined distance from a location pointed to by a read pointer associated with the second FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer, to effectuate a tail flush of said second FIPO storage structure.

54. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet write drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is no longer in the second FIFO storage structure, and

if so, reloads a write pointer associated with the second FIFO storage structure with an address that is of a first predetermined distance from a location pointed to by a read pointer associated with the second FIFO storage structure, and

writes an EOP at the location being pointed to by the reloaded write pointer,

to effectuate a tail flush of said second FIPO storage structure.

55. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet read drop logic, which, in response to an underflow condition of said second FIFO storage structure, while operating under a first protocol, multiplexes an EOP into said plurality of egress packets to denote to a downstream processor that a current egress packet is bad, to effectuate a head flush of said second FIPO storage structure.

56. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped is still in the process of being read out of the second FIFO storage structure, and

if so, invalidating remaining words of the egress packet,

to effectuate a head flush of said second FIPO storage structure.

57. The apparatus of claim 37, wherein said undiverted egress packet drop logic comprises undiverted egress packet read drop logic, which, in response to a drop egress packet control signal, while operating under a first protocol,

determines whether a SOP of an egress packet to be dropped has already been read out of the second FIFO storage structure, and

if so, invalidating an EOP indicator of a current word,

to effectuate a head flush of said second FIPO storage structure.

58. The apparatus of claim 37, wherein said buffering structure further comprises

a third FIFO storage structure coupled to said first ingress/egress point to stage diverted ones of said plurality of egress packets; and

diverted egress packet write drop logic coupled to the third FIFO storage structure to effectuate a tail flush of the third FIFO storage structure.

59. The apparatus of claim 58, wherein said diverted egress packet write drop logic effectuates a tail flush of the third FIFO storage structure in substantially the same manner as said undiverted egress packet write drop logic effectuates a tail flush of the second FIFO storage structure.

60. An optical networking module comprising:

an optical component to send and receive optical signals encoded with data transmitted through a coupled optical medium;

an optical-electrical component coupled to the optical component to encode digital data onto optical signals and to decode encoded digital data on optical signals back into their digital forms;

a data link/physical layer processing unit, coupled to the optical-electrical component and to a packet source/sink, including a buffering structure having at least a first FIFO storage structure to stage a selected one of undiverted ones of a plurality of ingress packets and undvierted ones of a plurality of egress packets, and

first associated packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flush of the first FIFO storage structure; and

a body encasing said optical component, said optical-electrical component, and said data link/physical processing unit as a single module.

61. The optical networking module of claim 60, wherein said first associated packet drop logic comprises write drop logic coupled to an input end of the first FIFO storage structure and equipped to perform a tail flush of the first FIFO storage structure under a first plurality of conditions, and read drop logic coupled to an output end of the first FIFO storage structure and equipped to perform a head flush of the first FIFO storage structure under a first plurality of conditions.

62. The optical networking module of claim 60, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage undiverted ones of a plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flush of the second FIFO storage structure.

63. The optical networking module of claim 60, wherein said first FIFO storage structure stages undiverted ones of a plurality of egress packets, and said buffering stage further comprises at least a second FIFO structure to stage diverted ones of the plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate tail flushes of the second FIFO storage structure.

64. The optical networking module of claim 60, wherein said first FIFO storage structure stages undiverted ones of a plurality of egress packets, and said buffering stage further comprises at least a second FIFO structure to stage insertion ones of the plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate head flushes of the second FIFO storage structure.

65. The optical networking module of claim 60, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage diverted ones of the plurality of ingress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate tail flushes of the second FIFO storage structure.

66. The optical networking module of claim 60, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage insertion ones of the plurality of ingress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate head flushes of the second FIFO storage structure.

67. The optical network module of claim 60, wherein said optical and optical-electrical components, said data link/physical layer processing unit are all designed to support data rates of at least 10GB/s.

68. The optical network module of claim 60, wherein said data link/physical layer processing unit is a multi-protocol processor that supports a plurality of datacom and telecom protocols.

69. A multi-protocol processor comprising:

a plurality of I/O interfaces to facilitate selective optical-electrical trafficking of data transmitted in accordance with a selected one of a plurality of datacom and telecom protocols;

a plurality of data link and physical sub-layer processing units selectively coupled to each other and to the I/O interfaces to be selectively employed in combination to perform selected data link and physical sub-layer processing on egress as well as ingress ones of said data, in accordance with said selected one of said plurality of protocols; and

a buffering structure coupled to at least a system-side one of said I/O interfaces and a media processing one of said data link and physical sub-layer processing units, including at least a first FIFO storage structure to stage a selected one of undiverted ones of a plurality of ingress packets and undvierted ones of a plurality of egress packets, and first associated packet drop logic coupled to the first FIFO storage structure to selectively effectuate head or tail flush of the first FIFO storage structure.

70. The multi-protocol processor of claim 69, wherein said first associated packet drop logic comprises write drop logic coupled to an input end of the first FIFO storage structure and equipped to perform a tail flush of the first FIFO storage structure under a first plurality of conditions, and read drop logic coupled to an output end of the first FIFO storage structure and equipped to perform a head flush of the first FIFO storage structure under a first plurality of conditions.

71. The multi-protocol processor of claim 69, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage undiverted ones of a plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to selectively effectuate head or tail flush of the second FIFO storage structure.

72. The multi-protocol processor of claim 69, wherein said first FIFO storage structure stages undiverted ones of a plurality of egress packets, and said buffering stage further comprises at least a second FIFO structure to stage diverted ones of the plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate tail flushes of the second FIFO storage structure.

73. The multi-protocol processor of claim 69, wherein said first FIFO storage structure stages undiverted ones of a plurality of egress packets, and said buffering stage further comprises at least a second FIFO structure to stage insertion ones of the plurality of egress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate head flushes of the second FIFO storage structure.

74. The multi-protocol processor of claim 69, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage diverted ones of the plurality of ingress packets, and second associated packet drop logic coupled to

the second FIFO storage structure to effectuate tail flushes of the second FIFO storage structure.

75. The multi-protocol processor of claim 69, wherein said first FIFO storage structure stages undiverted ones of a plurality of ingress packets, and said buffering stage further comprises at least a second FIFO structure to stage insertion ones of the plurality of ingress packets, and second associated packet drop logic coupled to the second FIFO storage structure to effectuate head flushes of the second FIFO storage structure.

76. A buffering structure comprising:

a first FIFO storage structure coupled to a system-side interface at an input end and to a network interface at an output end to stage undiverted ones of egress packets;

a second FIFO storage structure coupled to the system-side interface to stage diverted ones of egress packets;

a third FIFO storage structure to the network interface to stage insertion ones of egress packets;

first write packet drop logic coupled to the first FIFO storage structure to perform tail flushes of the first FIFO storage structure;

second write packet drop logic coupled to the second FIFO storage structure to perform tail flushes of the second FIFO storage structure; and

first read packet drop logic coupled to the first FIFO storage structure to perform head flushes of the first FIFO storage structure.

77. The buffering structure of claim 76, wherein said buffering structure further comprises

a fourth FIFO storage structure coupled to the network interface at one end and to the system-side interface at another end to stage undiverted ones of ingress packets;

a fifth FIFO storage structure coupled to the network interface to stage diverted ones of ingress packets;

third write packet drop logic coupled to the fourth FIFO storage structure to perform tail flushes of the fourth FIFO storage structure; and

fourth write packet drop logic coupled to the fifth FIFO storage structure to perform tail flushes of the fifth FIFO storage structure.

78. The buffering structure of claim 76, wherein said buffering structure further comprises

a fourth FIFO storage structure coupled to the network interface at one end and to the system-side interface at another end to stage undiverted ones of ingress packets;

third write packet drop logic coupled to the fourth FIFO storage structure to perform tail flushes of the fourth FIFO storage structure; and

second read packet drop logic coupled to the fourth FIFO storage structure to perform head flushes of the fourth FIFO storage structure.

79. A buffering structure comprising:

a first FIFO storage structure coupled to a network interface at an input end and to a system-side interface at an output end to stage undiverted ones of ingress packets;

a second FIFO storage structure coupled to the network interface to stage diverted ones of ingress packets;

a third FIFO storage structure to the system-side interface to stage insertion ones of ingress packets;

first write packet drop logic coupled to the first FIFO storage structure to perform tail flushes of the first FIFO storage structure;

second write packet drop logic coupled to the second FIFO storage structure to perform tail flushes of the second FIFO storage structure; and

first read packet drop logic coupled to the first FIFO storage structure to perform head flushes of the first FIFO storage structure.

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